IEEE Computer Society Annual Symposium on VLSI (Virtual)
Tampa, Florida, USA, July 7-9 2021

Program Schedule

Day 1 - July 7 All times are in **EDT** (Eastern Daylight Time = UTC – 4hours)			
11:30 – 11:45 am	ISVLSI 2021 Opening Remarks		
11:45 – 12:45 pm	Keynote 1 – *Reimagining Digital Design* Mr. Serge Leef Program Manager, DARPA		
12:45 – 01:00 pm	Break		
01:00 – 01:50 pm	Session 1 – Circuits, Reliability, and Fault-Tolerance (CRT)	Session 2 – Computer Aided Design and Verification (CAD)	Session 3 – Digital Circuits and FPGA based Designs (DCF)
01:50 – 02:00 pm	Break		
02:00 – 03:00 pm	Keynote 2 – *The Dual Role of Technology in Addressing Climate Change* Dr. Tamar Eilam IBM Fellow, IBM T. J. Watson Research Center		
3:05 – 3:30 pm	Break		
3:30 – 4:20 pm	Session 4 – Emerging and Post CMOS Technologies (EPT)	Session 5 – SDS-1 System Design and Security (SDS)	Session 6 – VLSI for Applied and Future Computing (AFC)

Day 2 - July 8 All times are in US **EDT** (Eastern Daylight Time = UTC – 4hours)	
11:30 – 12:30 pm	Session 7 - Best Paper Presentations
12:30 – 12:45 pm	Break
12:45 – 01:45 pm	Keynote 3 – *Optimal Layout Synthesis for Quantum Computing* Prof. Jason Cong Volgenau Chair for Engineering Excellence Professor CS Department, UCLA
01:45 – 02:00 pm	Break
02:00 – 03:00 pm	Panel -*"IoT and AI Will Develop Revolutionary Solutions to Critical Global Problems: A Real Promise or Just a Hype?"*

	Moderator: Himanshu Thapliyal (UK) Panelists: Kemal Akkaya (FIU), Swarup Bhunia (UF), Juncao Li (Lime), Saraju Mohanty (UNT), and Dan Zhang (Google)		
03:00 – 03:15 pm	Break		
03:15 – 4:05 pm	Session 8 –Special Session: Efficient Accelerator Design on Reconfigurable Architecture	Session 9 – Special Session: Side Channel Attack/Protections on Emerging Technology	Session 10 – AFC-2: VLSI for Applied and Future Computing (AFC)
04:05 – 04:15 pm	Break		
04:15 – 05:15 pm	Session 11 –Special Session: FPGA Security in the Era of Machine Learning and Cloud Computing	Session 12 – Special Session: Hardware Design of Emerging Electronics	Session 13 – SDS-2 System Design and Security (SDS)

Day 3 - July 9 All times are in US **EDT** (Eastern Daylight Time = UTC – 4hours)	
11:30 – 12:30 pm	Keynote 4 – *Transforming Chip Design in the Age of Machine Learning* Dr. Dan Zhang, Google
12:30 – 12:45 pm	Best Paper Award Presentations
12:45 – 01:45 pm	*Poster Session* Student Research Forum (SRF) & Research Demo Session (RDS)
01:45 – 02:00 pm	ISVLSI 2021 Closing Remarks
02:00 – 05:30 pm	Quantum Computing Workshop

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Program Schedule
Detailed Program

Day 1 - July 7
All times are in **EDT** (Eastern Daylight Time = UTC – 4hours)

11:30 – 11:45 am	ISVLSI 2021 Opening Remarks
11:45 – 12:45 pm	Keynote 1 – *Reimagining Digital Design* Speaker: Mr. Serge Leef, Program Manager, DARPA Chair: Sandip Ray, U of Florida
12:45 – 01:00 pm	Break (15 min)
01:00 – 01:35 pm	Session 1 – Circuits, Reliability, and Fault-Tolerance (CRT) Chair(s): S. R. Patri, NIT Warangal, India
01:00 pm	*A Fully Digital Foreground Calibration Technique of A Flash ADC* S. Chatterjee, M. Diamari, and S. Roy, IIIT Guwahati, India
01:10 pm	*An Adaptive Lockstep Architecture for Mixed-Criticality Systems* F. Kempf, T. Hartmann, S. Baehr, and J. Becker, KIT, Germany
01:20 pm	*Real-Time IC Aging Prediction via On-Chip Sensors* [1]K. Huang, [2]Md T. H. Anik, [1]X. Zhang, and [2]N. Karimi [1]San Diego State Univ., USA, [2]Univ. of Maryland Baltimore County, USA
01:30 pm	*A 1-V, 10-Bit, 250 MS/s, Current-Steering Segmented DAC for Video Applications,* S. C. Kumar, S. Kala, Y. B. N. Kumar, MH. Vasantha, NIT Goa, India
01:00 – 01:40 pm	Session 2 – Computer Aided Design and Verification (CAD) Chair(s): M. Velev, Aries Design Automation, USA
01:00 pm	*ILP-GRC: Integer Linear Programming-Based Global Routing With Cell Movement,* [1]T. A. Fontana, [2]E. Aghaeekiasaree, R. Netto, S. F. Almeida, U. Gandhi, A. F. Tabrizi, D. Westwick, [2]L. Behjat, and [1]J. Guntzel [1]UFSC Brazil, [2]Univ. of Calgary, Canada
01:10 pm	*A Comparative Study of Specification Mining Methods for SoC Communication Traces*

[1]M. R. Ahmed, [1]H. Zheng, [2]P. Mukherjee, [2]M. C. Ketkar, and [2]J. Yang
[1]Univ. of South Florida, [2]USA, Intel, USA

01:20 pm *Reverse Engineering Register to Variable Mapping in High-Level Synthesis*
M. Adem, R. Gupta, and C. Karfa, IIT Guwahati, India

01:30 pm *FPGA Resource and Performance Estimation for Convolutional Neural Networks*
M. Shahshahani and D. Bhatia, Univ. of Texas, Dallas, USA

01:00 – 01:45 pm Session 3 – Digital Circuits and FPGA based Designs (DCF)
Chairs: H. Zheng, University of South Florida
J. Dofe, California State University, Fullerton

01:00 pm Stochastic Number Generators With Minimum Probability Conversion Circuits
S. A. Salehi and C. Collinsworth, University of Kentucky, USA

01:10 pm *Counter Random Gradient Descent Bit-Flipping Decoder for LDPC Codes*
K. Deng, H. Cui, J. Lin, and Z. Wang, Nanjing University, China

01:20 pm *Depth Optimized Synthesis of Symmetric Boolean Functions*
[1]M. Schneiber, [2]S. Froehlich, and [2,3]R. Drechsler
[1]GRCAI GmBH, Germany, [2]Univ. of Bremen, Germany, [3]DFKI Germany

01:30 pm *A Multi-Context Neural Core Design for Reconfigurable Neuromorphic Arrays*
A. Foshie, N. Chakraborty, J. J. Murray VI, T. Fowler, and G. S. Rose
Univ. of Tennessee, Knoxville, USA

01:40 pm *A Terabit Hybrid FPGA-ASIC Platform for Switch Virtualization*
[1]M. Tirone, [1]R. Brum, [2]B. Zatt, [3]S. Pagliarini, [1]W. L. da Costa Cordeiro, and [1]J. Azambuja,
[1]FURGS, Brazil, [2]FUP, Brazil, [3]Tallinn Univ. of Technology, Estonia

1:50 – 02:00 pm Break

02:00 – 3:00 pm Keynote 2 - *The Dual Role of Technology in Addressing Climate Change*
Speaker: Dr. Tamar Eilam, IBM Fellow, IBM T. J. Watson Research Center
Chair: Dr. Aida Todri-Sanial, LIRMM

03:05 – 03:30 pm Break

03:30 – 04:10 pm Session 4 – Emerging and Post CMOS Technologies (EPT)
Chair(s): Sandeep Miryala, Brookhaven National Lab, USA

03:30 pm *Crosstalk Logic Circuits With Built-In Memory*
[1]M. Rahman, [2]N. Macha, and [1]P. Samant
[1]Univ. of Missouri-Kansas City, USA, [2]NVIDIA Corp., USA

03:40 pm *SpamHD: Efficient Text Spam Detection Using Brain-Inspired Hyperdimensional Computing*
R. Thapa, B. Lamichhane, D. Ma, and X. Jiao
Villanova University, USA

03:50 pm *HDXplore: Automated Differential Testing of Brain-Inspired Hyperdimensional Computing*
R. Thapa, D. Ma, and X. Jiao
Villanova University, USA

04:00 pm *BDD Variable Ordering for Minimizing Power Consumption of Optical Logic Circuits*
R. Matsuo and S. Minato,
Kyoto University, Japan

04:05 pm *Scaling Constraints for Memristor-Based Programmable Interconnect in Reconfigurable Computing Arrays*
J. J. Murray VI, A. Z. Foshie, M. S. Shawkat, and G. S. Rose,
Univ. of Tennessee, Knoxville, USA

03:30 – 04:20 pm Session 5 – SDS-1 System Design and Security (SDS)
Chairs: Q. Yu, University of New Hampshire, USA
M. Kermani, University of South Florida, USA

03:30 pm *Tile Architecture and Hardware Implementation for Computation in Memory*
M. Zahedi, R. van Duijnen, S. Wong, and S. Hamdioui
Delft Univ. of Technology (TU Delft), The Netherlands

03:40 pm *On Preventing SAT Attack With Decoy Key-Inputs*
Q-L. Nguyen, M-L. Flottes, S. Dupuis, and B. Rouzeyre
LIRMM, Univ. de Montpellier, France

03:50 pm *An Extensible Evaluation Platform for FPGA Bitstream Obfuscation Security*
S. Mahmud, B. Olney, and R. Karam
University of South Florida, USA

04:00 pm *Lorax: Machine Learning-Based Oracle Reconstruction With Minimal I/O Patterns*
[1]W. Zeng, [1]A. Davoodi, and [2]R. O. Topaloglu

[1]University of Wisconsin-Madison, USA, [2]IBM, USA

04:10 pm — *Towards Enhancing Power-Analysis Attack Resilience for Logic Locking Techniques*
Z. Zhang and Q. Yu
Univ. of New Hampshire, USA

03:30 – 04:20 pm — Session 6 – AFC-1 VLSI for Applied and Future Computing (AFC)
Chairs: R. Shafik, Newcastle University

03:30 pm — *Heartbeat Classification With Spiking Neural Networks on the Loihi Neuromorphic Processor*
K. R. Buettner and A. George
University of Pittsburgh, USA

03:40 pm — *A Reconfigurable Accelerator for Generative Adversarial Network Training Based on FPGA*
T. Yin, W. Mao, J. Lu, and Z. Wang
Nanjing University, China

03:50 pm — *Analog Circuit Implementation of Neural Networks for In-Sensor Computing*
J. Zhu, B. Chen, Z. Yang, L. Meng, and T. Ye
Southern Univ. of Science and Technology, China

04:00 pm — *Carry-Free Addition in Resistive RAM Array: N-Bit Addition in 22 Memory Cycles*
J. Reuben and D. Fey
Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

04:10 pm — *A Flexible In-Memory Computing Architecture for Heterogeneously Quantized CNNs*
F. Ponzina, M. Rios, G. Ansaloni, A. Levisse, and D. Atienza
EPFL, Switzerland

Day 2 - July 8
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11:30 – 12:30 pm — Session 7 – Best Paper Presentations
Chairs: J. Becker, KIT and S. Mohanty, UNT

11:30 am — *FPU Reduced Variable Precision in Time: Application to the Jacobi Iterative Method*
N. A. Said, M. Benabdenbi, and K Morin-Allory
Univ. of Grenoble Alpes, CNRS, Grenoble INP, TIMA, France

11:40 am *SkyBridge-3D-CMOS 2.0: IC Technology for Stacked-Transistor 3D ICs Beyond FinFETs*
S. Bhat, M. Li, S. Ghosh, S. Kulkarni, C Andras-Moritz,
Univ. of Massachusetts, Amherst, USA

11:50 am *PipeBSW: A Two-Stage Pipeline Structure for Banded Smith-Waterman Algorithm on FPGA*
L. Li, J. Lin, and Z. Wang, Nanjing University, China

12:00 pm *An In-Memory Analog Computing Co-Processor for Energy-Efficient CNN Inference on Mobile Devices*
[1]M. Elbtity, [2]A. Singh, [1]B. Reidy, [2]X. Guo, and [1]R. Zand
[1]Univ. of South Carolina, USA, [2]Lehigh Univ., USA,

12:10 pm *Dynamic Fault Tree Models for FPGA Fault Tolerance and Reliability*
[1]Y. Elderhalli, [2,3]N. Elaraby, [4]O. Hasan, [2]A. Jantsch, and [1]S. Tahar,
[1]Concordia Univ., Canada, [2]TU Wien, Austria, [3]CIC Egypt,
[4]NUST, Pakistan

12:20 pm *ATRIA: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-DRAM CNN Processing*
S. M. Shivanandamurthy, I. Thakkar, and S. A. Salehi
University of Kentucky, USA

12:30 – 12:45 am Break (15 min)

12:45 – 1:45 pm Keynote 3 – *Optimal Layout Synthesis for Quantum Computing*
Speaker: Prof. Jason Cong, Volgenau Chair for Engineering Excellence Professor, Computer Science Department, UCLA
Chair: Deming Chen, U of Illinois, Urbana-champaign

01:45 – 02:00 pm Break (15 min)

02:00 – 03:00 pm Panel -*"IoT and AI Will Develop Revolutionary Solutions to Critical Global Problems: A Real Promise or Just a Hype?"*
Moderator: Himanshu Thapliyal (UK)
Panelists: Kemal Akkaya (FIU), Swarup Bhunia (UF), Juncao Li (Lime), Saraju Mohanty (UNT), and Dan Zhang (Google)

03:00 – 03:15 pm Break (15 min)

03:15 – 04:05 pm **Session 8 – Special Session: Efficient Accelerator Design on Reconfigurable Architecture**
Chairs: W. Zhang, HKUST, Hong Kong
S. Katkoori, University of South Florida, USA

03:15 pm *DiCE-LSTM: An n-Dimensional Configurable and Efficient Architecture for LSTM Accelerator*
Z. Navabi, H. T. Asl, and M. S. Roodsari
University of Tehran, Iran

03:25 pm *Micro-Architecture Tuning for Dynamic Frequency Scaling in Coarse-Grain Runtime Reconfigurable Arrays With Adaptive Clock Domain Support*
Q. Si, Md Imtiaz Rashid, and B. C. Shafer
The University of Texas at Dallas, USA

03:35 pm *Low Bitwidth CNN Accelerator on FPGA Using Winograd and Block Floating Point Arithmetic*
[1]Z. Dong, [2]Y. Wong, and [2]W. Zhang
[1]HiSilicon, China, [2]HKUST, Hong Kong

03:45 pm *Custom Enhancements to Networked Processor Templates*
W. Luk and T. Todman
Imperial College, United Kingdom

03:55 pm *Analyzing the Design Space of Spatial Tensor Accelerators on FPGAs*
L. Jia, Z. Luo, L. Lu, and Y. Liang
Peking University, China

03:15 – 04:05 pm **Session 9 – Special Session: Side Channel Attack/Protections on Emerging Technology**
Chairs: Mike Borowczak, University of Wyoming, USA
Domenic Forte, University of Florida, USA

03:15 pm *Side-Channel Leakage Assessment Metrics: A Case Study of GIFT Block Ciphers*
[1]W. Unger, [2]L. Babinkostova, [1]M. Borowczak, and [3]R. Erbes
[1]University of Wyoming, USA, [2]Boise State University, USA, [3]Idaho National Laboratory, USA

03:25 pm *Stealing Model Parameters via Side Channel Power Attack*
S. Wolf, H. Hu, R. Cooley, and M. Borowczak
University of Wyoming, USA

03:35 pm *Security Capsules: An Architecture for Post-Silicon Security Assertion Validation for Systems-On-Chip*
S. Raja, P. Bhamidipati, X. Liu, and R. Vemuri
University of Cincinnati, USA

03:15 – 04:05 pm Session 10 – VLSI for Applied and Future Computing
Chairs: V. Ramnath, Oklahoma State University, USA

03:15 pm *An FPGA-Based Reconfigurable Accelerator for Low-Bit DNN Training*
H. Shao, J. Lu, J. Lin, Z. Wang
Nanjing University, China

03:25 pm *Accelerating Spectral Normalization for Enhancing Robustness of Deep Neural Networks*
Z. Pan and P. Mishra
University of Florida, USA

03:35 pm *A Microarchitecture Implementation Framework for Online Learning With Temporal Neural Networks*
[1]H. Nair, [1]J. Shen, and [2]J. E. Smith
[1]Carnegie Mellon University, USA, [2]University of Wisconsin, USA

04:05 – 04:15 pm Break (10 min)

04:15 – 05:05 pm Session 11 - Special Session: FPGA Security in the Era of Machine Learning and Cloud Computing
Chairs: Q. Yu, University of New Hampshire, USA
J. Hu, University of Pittsburgh, USA

04:15 pm *Neural Networks as a Side-Channel Countermeasure: Challenges and Opportunities*
J. Krautter and M. Tahoori
Karlsruhe Institute of Technology (KIT), Germany

04:25 pm *New Security Threats on FPGAs: From FPGA Design Tools Perspective*
S. Sunkavalli, Z. Zhang, and Q. Yu
University of New Hampshire, USA

04:35 pm *A Survey of Recent Attacks and Mitigation on FPGA Systems*
S. Duan, W. Wang, Y. Luo, and X. Xu
Northeastern University, USA

04:45 pm *A Security Architecture for Domain Isolation in Multi-Tenant Cloud FPGAs*
J. M. Mbongue, S. K. Saha, and C. Bobda
University of Florida, Gainesville, USA

04:55 pm *Efficient Hardware Implementation of PQC Primitives and PQC Algorithms Using High-Level Synthesis*
D. Soni and R. Karri

New York University, USA

04:15 – 05:25 pm **Session 12 - Special Session: Hardware Design of Emerging Electronics**
Chairs: H. Thapliyal, University of Kentucky, USA
A. Roohi, University of Nebraska Lincoln, USA

04:15 pm *A Reconfigurable and Compact Spin-Based Analog Block for Generalizable Nth Power and Root Computation*
A. Tatulian and R. DeMara
University of Central Florida, USA

04:25 pm *Design of an Approximate FFT Processor Based on Approximate Complex Multipliers*
J. Du, K. Chen, P. Yin, C. Yan, and W. Liu
Nanjing University of Aeronautics and Astronautics, China

04:35 pm *Low-Energy and CPA-Resistant Adiabatic CMOS/MTJ Logic for IoT Devices*
Z. Kahleifeh and H. Thapliyal
University of Kentucky, USA

04:45 pm *Proposal of A Novel Hybrid NAND-Like MRAM/DRAM Memory Architecture*
K. He, Z. Yang, Z. Yu, J. Zhi, Z. Wang, Y. Wang
Beihang University, China

04:55 pm *Oscillatory Neural Networks for Edge AI Computing*
C.Deacour, S. Carapezzi, M. Abernot, G. Boschetto, N. Azemard, J. Salles, T. Gil, and A. Todri-Sanial
LIRMM, University of Montpellier, CRNS, France

05:05 pm *EQUAL: Efficient QUasi Adiabatic Logic for Enhanced Side-Channel Resistance*
K. Dhananjay and E. Salman
Stony Brook University, USA

05:15 pm *Scalable Resonant Power Clock Generation for Adiabatic Logic Design*
B. Taskin, R. Kuttappa, L. Filippini, and N. Sica
Drexel University, USA

04:15 – 04:55 pm Session 13 – Secure Design and Security
Chairs: R. Reis, UFRGS, Brazil
R. Karam, University of South Florida, USA

04:15 pm *HEXON: Protecting Firmware Using Hardware-Assisted Execution-Level Obfuscation*
[1]M. M. Hossain, [1]S. Mohammad, [1]J. Vosatka, [2]J. Allen, [2]M. Allen,
[1]F. Farahmandi, [1]F. Rahman, and [1]M. Tehranipoor
[1]University of Florida, USA, [2]AFRL, Eglin Air Force Base, FL, USA

04:25 pm *Enhancing PRESENT-80 and Substitution-Permutation Network Cipher Security With Dynamic "Keyed" Permutation Networks*
M. D. Lewandowski and S. Katkoori
University of South Florida, USA

04:35 pm *Countering PUF Modeling Attacks Through Adversarial Machine Learning*
M. Ebrahimabadi, W. Lalouani, M. Younis, and N. Karimi
University of Maryland Baltimore County, USA

04:45 pm *LightRoaD: Lightweight Rowhammer Attack Detector*
[1]M. Taouil, [1]C. R. W. Reinbrecht, [1]S. Hamdioui, and [2]J. Sepulveda
[1]Delft University of Technology, The Netherlands, [2]TU Munich, Germany

04:50 pm *Minimized Region of Path-Search Algorithm for ASIP-Based Connection Allocator in NoCs*
S. Nam, E. Matus, G. Fettweis,
Technical university of Dresden, Dresden, Germany

Day 3 - July 9
All times are in US **EDT** (Eastern Daylight Time = UTC – 4hours)

11:30 – 12:30 pm Keynote 4 – *Transforming Chip Design in the Age of Machine Learning*
Speaker: Dr. Dan Zhang, Google
Chair: Hao Zheng, University of South Florida

12:30 – 12:45 pm Best Paper Award Presentations

12:45 – 01:45 pm Student Research Forum (SRF)
Chairs: R. Karam, University of South Florida, USA

Improved Polygon Method for HIL Simulations in Real Time
M. Yushkova, A. Sanchez, and A. de Castro
Univ. Autonoma de Madrid, Spain

Machine Learning for VLSI CAD: A Case Study in On-Chip Power Grid Design
S. Dey, IIT Guwahati, India

MCTS-Based Synthesis Towards Efficient Approximate Accelerators
M. Awais and M. Platzner
Paderborn University, Germany

Wearable Health Monitoring System for Older Adults in a Smart Home Environment
R. Nath land H. Thapliyal
University of Kentucky, USA

12:45 – 01:45 pm Research Demo Session (RDS)
Chairs: S. A. Islam, Univ. of Texas Rio Grande Valley, USA

Implementation of a QPSK Symbol Synchronizer in Xilinx System Generator
B. Comar, US DoD, USA

Efficient Hardware Implementation of Convolution Layers Using Multiply-Accumulate Blocks
M. E. Nojehdeh, S. Parvin, and M. Altun
Istanbul Technical University, Turkey

A Study on Hardware-Aware Training Techniques for Feedforward Artificial Neural Networks
S. Parvin and M. Altun
Istanbul Technical University, Turkey

Hardware Trojan Classification at Gate-Level Netlists Based on Area and Power Machine Learning Analysis
K. Liakos, G. Georgakilas, and F. Plessas
University of Thessaly, Greece

FPGA Implementation of High Speed Anti-Notch Lattice Filter for Exon Region Identification in Eukaryotic Genes
[1]V. Pathak, [1]S. J. Nanda, [1]A. Joshi, and [2]S. Sahu
[1]MNIT Jaipur, India, [2]BIT Mesra, India

01:45 – 02:00 pm ISVLSI 2021 Closing Remarks

02:00 – 05:30 pm Quantum Computing Workshop

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